ABSTRACT

A method and system for automatically building a bit order data structure of configuration bits for a programmable logic device. One embodiment of the present invention first identifies a plurality of memory cells in a hierarchical schematic representation of the programmable device. Next, this embodiment determines a plurality of addresses corresponding to the plurality of memory cells. This embodiment next determines a plurality of logical names for the plurality of memory cells. Then, based on an order in which the plurality of addresses are to be loaded into the programmable logic device, this embodiment orders the plurality of logical names for the plurality of memory cells. Another embodiment first accesses a database comprising a plurality of logical names corresponding to a plurality of addresses. Then, this embodiment accesses a database specifying an order in which the plurality of addresses are to be loaded into the programmable logic device. Next, this embodiment orders the plurality of logical names based on the order specified in the database from the previous step.